UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,998	10/21/2003	Chee Choong Kooi	P17171	4865

28062 7590 12/13/2005

BUCKLEY, MASCHOFF, TALWALKAR LLC
5 ELM STREET
NEW CANAAN, CT 06840

EXAMINER	
CARPIO, IVAN HERNAN	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

4K

Office Action Summary	Application No.	Applicant(s)	
	10/689,998	KOOI ET AL.	
	Examiner	Art Unit	
	Ivan H. Carpio	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 10-21-03 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1-3 and 11-13 rejected under 35 U.S.C. 102(e) as being anticipated by Shim (US Patent 6599779).

With respect to claim 1 Shim teaches an apparatus comprising: an integrated circuit die (Fig.2, element 12); an integrated circuit package (Fig.2, element 13) coupled to a first face of the integrated circuit die; mold compound (Fig. 2, element 34) in contact with the integrated circuit die and the integrated circuit package; and an overlayer (Fig. 2, element 19) coupled to the mold compound and to a second face of the integrated circuit die.

With respect to claim 2 and with all the limitations of claim 1, Shim teaches underfill material (Fig.2, element 18) disposed between the integrated circuit die and the integrated circuit package.

With respect to claim 3 and with all the limitations of claim 1, Shim teaches that the overlayer comprises thermally conductive material (column 3, line 64).

With respect to claim 11 Shim teaches a method comprising: placing an overlayer (Fig.2, element 19) in contact with mold compound (Fig. 2, element 34) and a first face of an integrated circuit die (Fig.2, element 12), wherein a second face of the integrated circuit die is coupled to an integrated circuit package (Fig. 2, element 13), and wherein the mold compound is in contact with the integrated circuit die and the integrated circuit package.

With respect to claim 12 and with all the limitations of claim 11, Shim teaches singulating (Fig.2) one of the plurality of integrated circuit die and a respective mounting location of the integrated package substrate.

With respect to claim 13 and with all the limitations of claim 11, Shim teaches that the overlayer comprises thermally conductive material (column 3, line 64).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shim.

With respect to claim 6 Shim teaches all of the limitations including integrated circuit package substrate (Fig.2, element 13); an integrated circuit die (Fig.2, element 12), a first face of the integrated circuit die attached to the integrated circuit package

substrate; and mold compound (Fig.2, element 34) in contact with the integrated circuit die and the integrated circuit package substrate; and an overlayer (Fig.2, element 19) coupled to the mold compound and to a second face of the integrated circuit die. Shim does not teach a plurality of integrated circuit die each with the same configuration as described above. It is well known in the art to have a plurality of integrated circuit die on an integrated circuit substrate and several benefits for doing so. Motherboards have several different IC die on a substrate each of which performs different functions and which in unison perform desired functions of information processing. In the manufacturing of integrated circuit packages there are many identical IC die on a substrate for the purpose of redundancy and manufacturing efficiency. It would have been obvious to have a plurality of integrated circuit die on an integrated circuit package substrate with the same configuration as described by Shim for the purpose of either performing desired processing or manufacturing integrated circuit packages efficiently. With respect to the latter, it has been held that mere duplication of the essential working parts of a device involves only routing skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.*

With respect to claim 7 and with all the limitations of claim 6, Shim teaches underfill material (Fig.2, element 18) disposed between the first face of each of the plurality of integrated circuit die and the integrated circuit package substrate.

With respect to claim 8 and with all the limitations of claim 6, Shim teaches that the overlayer comprises thermally conductive material (column 3, line 64).

With respect to claims 4,5,9,10,14 and 15 Shim teaches all of the limitations except that the overlayer is a cured die attach film or paste. The particular material used as the overlayer depends on several factors such as the total heat produced by the IC die as well as cost considerations. It would have been obvious to one of ordinary skill in the art at the time of the invention to choose any suitable material for the overlayer, including cured attach film or paste, for the purpose of fulfilling needed properties and cost specifications. Furthermore it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.*

Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shim in view of Bhattacharyya (US Patent 6713810)

Bhattacharyya teaches all of the limitations of claims 16-18 including a microprocessor (Fig. 12, element 406) electrically coupled to a double data rate memory (Fig. 12, element 408, column 15, lines 65) and electrically coupled to a motherboard (Fig. 12, element 404). Bhattacharyya does not teach the specifics of the microprocessor such as a mold compound in contact with the integrated circuit die and the integrated circuit package and a thermally conductive overlayer coupled to the mold compound and to a second face of the integrated circuit die. Shim teaches an integrated circuit die (Fig.2, element 12), an integrated circuit package (Fig.2, element 13) coupled to a first face of the integrated circuit die, mold compound (Fig.2, element 34) in contact with the integrated circuit die and the integrated circuit package and a thermally

conductive overlayer (Fig.2, element 19, column 3, line 64) coupled to the mold compound and to a second face of the integrated circuit die. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the specific configuration of the IC chip, taught by Shim, for the microprocessor and system, taught by Bhattacharyya, for the benefit of improved heat dissipation and shielding (Shim column 1, lines 10-23).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ivan H. Carpio whose telephone number is 571-272-8396. The examiner can normally be reached on M-R 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KAMAND CUNEO
ERVISORY PATENT EXAMINER
NOLOGY CENTER 2800

IC